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FME/MS/SFDAC1E/UM_1/4133

DK86061-3 12-bit 400MSa/s DAC Evaluation Board

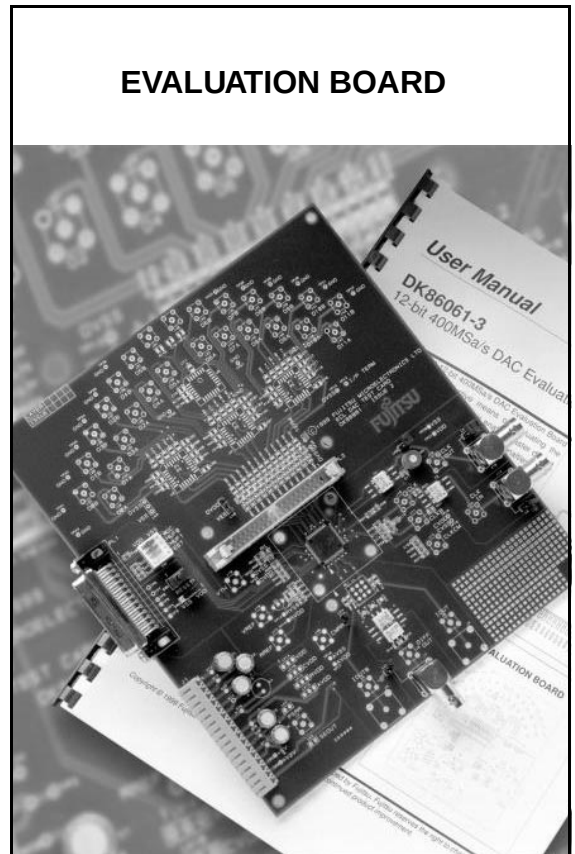
Fujitsu's DK86061-3 12-bit 400MSa/s DAC Evaluation Board provides a simple and effective means of evaluating the MB86061 12-bit 400MSa/s DAC. This enables faster device evaluation without incurring the time and cost penalties of in-house PCB design and manufacture.

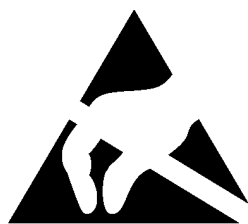
The board provides a complete evaluation environment for the DAC device. A selectable single-ended or transformer-coupled differential analog output interface is provided on-board to simplify integration into target application and development environments. The clock is sourced from a transformer coupled RF source. 12-bit ECL data is input via a 40way IDC header, or optional SMA/SMB connectors.

The MB86061 device is a single 12-bit DAC enclosed in a 64 pin QFP package with a 0.65mm pin pitch.

Features

- 12-bit ECL data input via a choice of connectors
- Transformer-coupled differential output via BNC
- Transformer-coupled RF clock input via BNC
- Requires DC power supplies of +3.3V and -2V





CAUTION

ELECTROSTATIC DISCHARGE SENSITIVE DEVICE

High electrostatic charges can accumulate in the human body and discharge without detection. Ensure proper ESD procedures are followed when handling this device.

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DK86061-3 12-bit 400MSa/s DAC Evaluation Board

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1 Overview

The DK86061-3 evaluation board allows users to evaluate and demonstrate the different operational modes of the MB86061 12-bit 400MSa/s DAC. The evaluation board consists of an MB86061 device with support circuitry for single-ended or differential analog output interfaces, a clock input interface and a clock output interface. This will enable simple connection of measurement equipment. For convenience customer evaluation boards have been configured using soldered zero-ohm links for transformer-coupled differential output only.

The ECL input data interface has a 40way IDC header, with selectable termination to VEE or DVSS. Separate SMA/SMB connectors for individual data bit connections are also available (but not normally fitted), with selectable termination to VEE or DVSS. Provision is made to multiplex data onto the input data interface from two speed limited but phase adjustable data generators. For this a second set of SMA/SMB connectors (again not normally fitted - SMA not recommended due to insufficient space to rotate the body) are also available. The setup of the device is controlled by on-board DIP switches, but these controls can be accessed and overridden via a male D type connector if remote control is required.

The evaluation board has been designed to address requirements of both automatic and conventional bench testing. Standard evaluation boards feature a simplified build state where certain components and connectors are omitted. These omissions are documented in Appendix A with the evaluation board schematics.

This User Manual is intended to document the DK86061-3 Development Kit PCB titled 'MB86061 DAC TEST CARD - ISSUE 3' only.

2 Evaluation Board

2.1 Power Supply

The DK86061-3 evaluation board requires two low voltage DC supplies, and a number of other low voltage DC supplies depending upon build configuration (marked †). A cable mounting socket suitable for mating with the PCB mounted power plug is supplied with the development board. Additional sockets, type Weidmüller BL3.5/16 may be obtained from RS Components (<http://rswww.com>), Stock no. 216-2683. The power should be connected to the board via this connector, as shown in Figure 2.1. Flexible cable of 16 - 28 AWG, 0.5 - 1.5mm² should be used.

The format of the power connector is common across Fujitsu's DAC Development Kit range. Some of the supply pins are connected to test points for convenience if the user requires supplies for the prototype area.

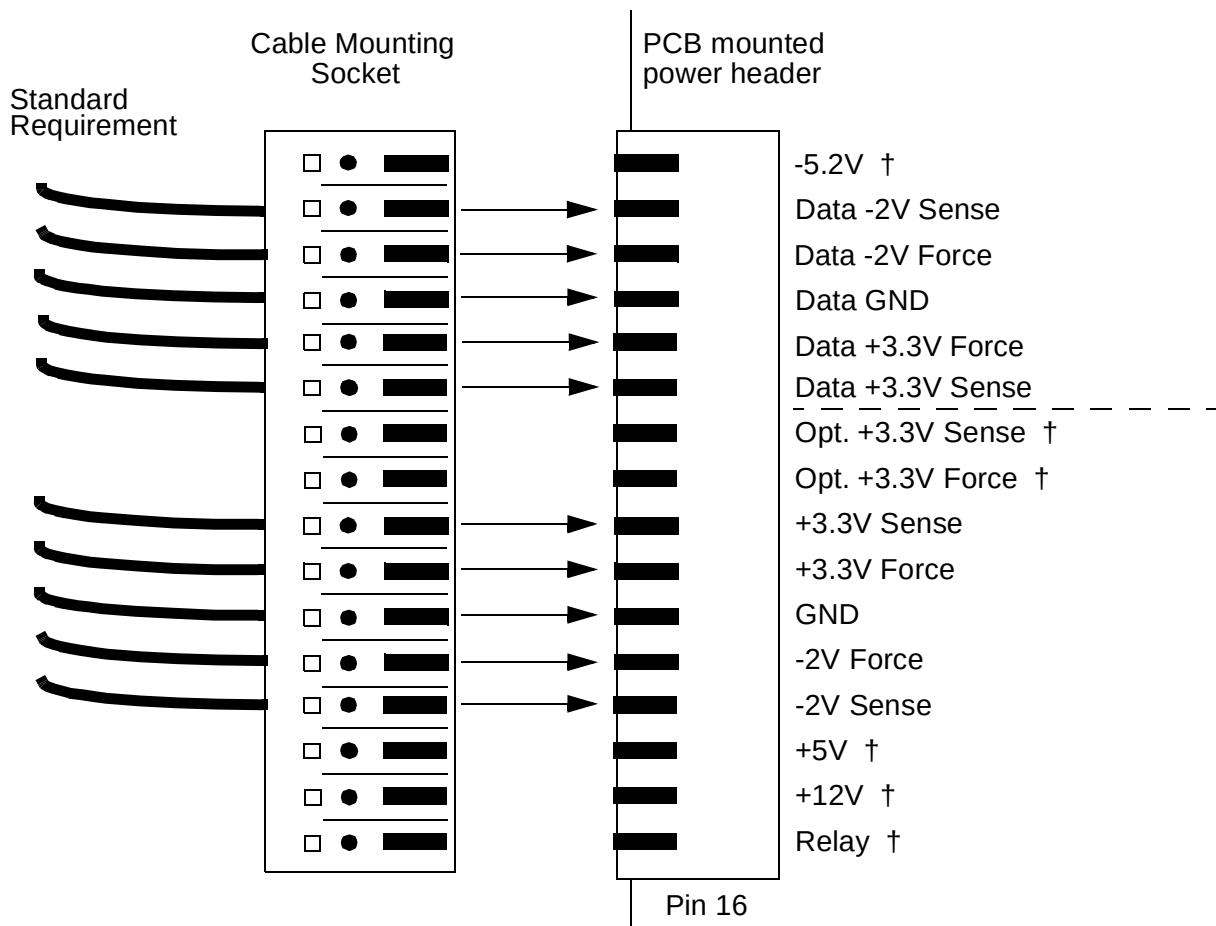


Figure 2.1: Power Connections

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2.2 Board and Interface Controls

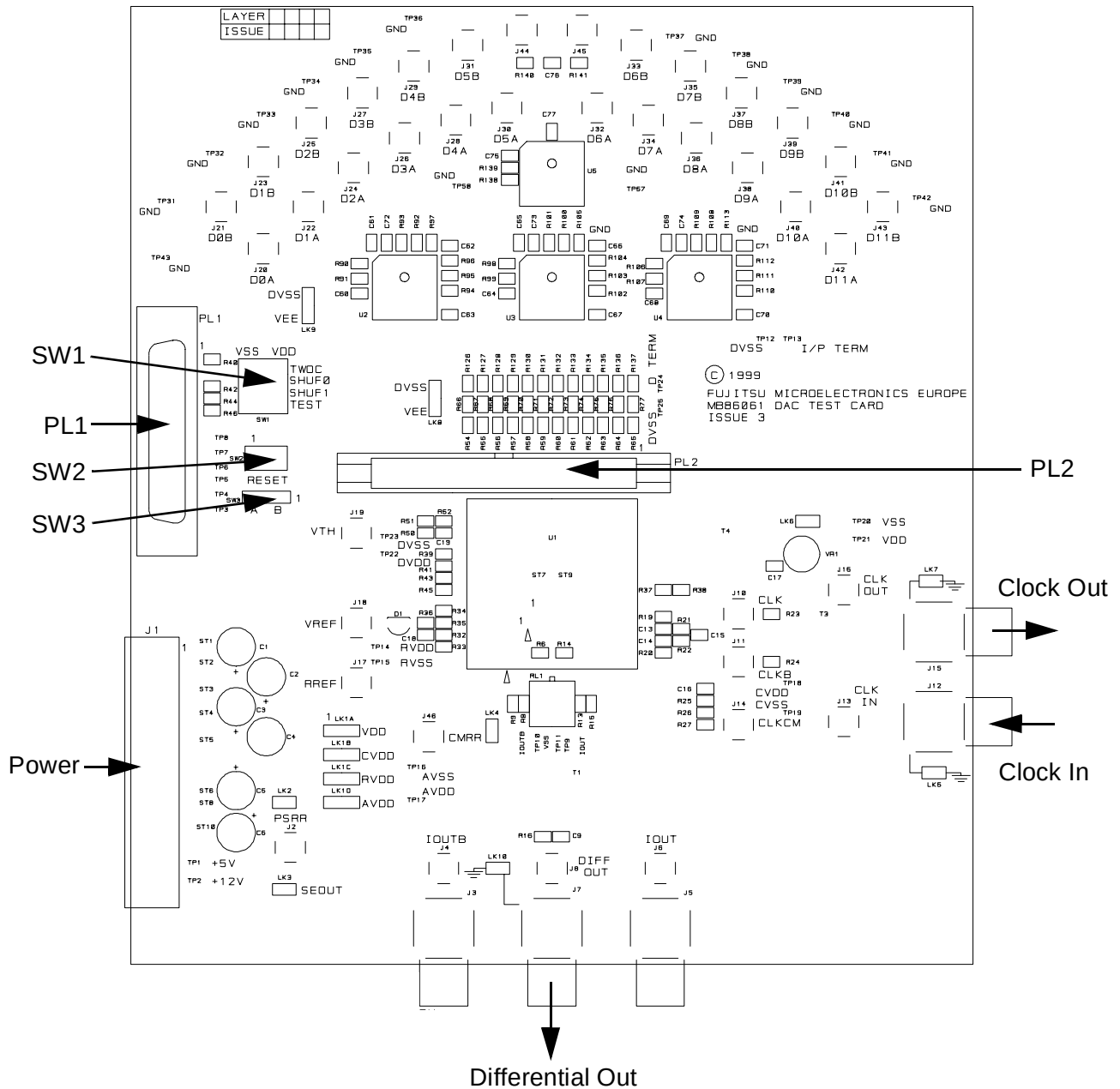


Figure 2.2: Evaluation Board Component Side Layout

2.2.1 Switches

There are several control switches on the evaluation board, as shown in Figure 2.2. Switch ids are marked on the board silk screen.

Table 1: Switch 1 Settings

Switch	Mode / Function	Settings
SW1[1] (TWOC)	Offset binary input data	VSS
	2's Compliment input data	VDD
SW1[2:3] (SHUF0, SHUF1)	Segment Shuffling disabled	VSS, VSS
	Random - every 4 cycles	VDD, VSS
	Random - every 8 cycles	VSS, VDD
	Random - every 16 cycles	VDD, VDD
SW1[4] (TEST)	Factory Use Only	VSS

Table 2: Switch 2 Settings

Switch	Mode / Function	Setting
SW2	Device Reset	Push to Reset

Table 3: Switch 3 Settings

Switch	Mode / Function	Setting
SW3	Device in forced RESET mode	B
	Device in normal operating mode	A

Note: SW1 may appear to malfunction if pressure is placed on the slider when in either the left or right position. In this case the DAC control pin will be floating.

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2.2.2 Jumper Links

Table 4: Jumper Links

Link Name	Mode / Function	Setting
LK1A† (VDD)	Optional supply used for VDD	1 to 2 linked
	Common supply used for VDD	2 to 3 linked
LK1B† (CVDD)	Optional supply used for CVDD	1 to 2 linked
	Common supply used for CVDD	2 to 3 linked
LK1C† (RVDD)	Optional supply used for RVDD	1 to 2 linked
	Common supply used for RVDD	2 to 3 linked
LK1D† (AVDD)	Optional supply used for AVDD	1 to 2 linked
	Common supply used for AVDD	2 to 3 linked
LK2† (PSRR)	Power supply ripple rejection disabled	Linked
	Power supply ripple rejection enabled	Not Linked
LK3‡ (SEOUT)	Select single-ended output	Linked
	Select differential output	Not linked
LK4 (CMRR)	Centre tap of T1 linked to AVSS	Linked
	Centre tap of T1 decoupled to AVSS	Not linked
LK5	CLK IN Ground linked to CVSS	Linked
	CLK IN Ground floating	Not Linked
LK6	CLK OUT biasing enabled	Linked
	CLK OUT biasing disabled	Not Linked
LK7	CLK OUT Ground linked to VSS	Linked
	CLK OUT Ground floating	Not Linked
LK8	DAC input terminated to DVSS	1 to 2 Linked
	DAC input terminated to VEE	2 to 3 Linked
LK9	Multiplexer data input terminated to DVSS	1 to 2 Linked
	Multiplexer data input terminated to VEE	2 to 3 Linked
LK10	DIFF OUT Ground linked to AVSS	Linked
	DIFF OUT Ground floating	Not Linked

Note: Bold type indicates default jumper settings.

† Standard Evaluation Kits are not configured to use the optional power supply. LK1 & LK2 are not used.

‡ Standard Evaluation Kits are configured for Differential output. LK3 is not used.

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3 Getting Started

This Chapter documents the basic steps to powering up and starting to use the DK86061-3 Evaluation Board. Component references may be cross-referenced with the component overlay in Appendix B.

Step 1. Configure board for data input format

The data input format must be configured to either Offset Binary or 2's Complement. Use configuration switch SW1[1] to select.

The device control signals should be set to the default conditions shown in Section 2.2. Use configuration switch SW1 to select.

Jumper links LK4 to LK7 inclusive, and LK10, should be 'Not linked', and LK8 and LK9 should be set to '2 to 3' linked. Switch SW3 should be set to position 'A'.

Step 2. Connect data input & analog output connectors to the board

The input data should be connected via the 40 way IDC header PL1, or if fitted the SMA/SMB connectors J20 to J42 inclusive (evens only). See Table C1: for the pin description of the IDC header.

The output is provided as a transformer-coupled differential signal, via a BNC connector.

- Differential Output signal (J7). (50 Ω source resistance)
The DAC is coupled to a single output connector using a transmission line and a 1:1 balun transformer. Signal swing is $\pm 0.5V$ with a high impedance load, or $\pm 0.25V$ with an external 50 Ω load. For sinusoidal signals, this corresponds to approximately -2dBm into a 50 Ω external load.

Step 3. Connect clock

The clock input is provided to the device through a transmission line transformer, via a BNC connector.

- RF clock (J12). (50 Ω input impedance)
The DAC is coupled to a single input connector using a transmission line transformer. Sine wave or square wave input signals between -10dBm and +10dBm are acceptable, depending on clock frequency and required output jitter / phase noise.

Step 4. Connect power header to power supplies

Ensure that the power supplies are connected according to Figure 2.1. Connect the power header to the board and turn power supplies on.

Step 5. Press Reset

Press the Reset button to ensure that the device is in the correct operating condition. Press Reset every time a configuration change is made.

4 Testing

This section provides a brief introduction to testing with the DK86061-3 12-bit 400MSa/s DAC Evaluation Board.

The MB86061 incorporates a 12-bit, 400MSa/s digital to analog converter designed to give excellent SFDR performance. Traditional 12-bit converters have been speed limited, in particular when considering CMOS solutions, and applications have tended to be limited to around 100MSa/s. In certain applications it is now possible to consider using the MB86061 with a 400MSa/s DAC conversion rate, even though the generated signal band may only be, for example, up to 40MHz or less. In theory a 100MSa/s converter would be sufficient to reproduce this 40MHz signal band, but according to Nyquist the converters performance will tend to be limited due to step-size and $\sin x/x$ roll-off, as a result of the converters sample & hold output stage. A 400MSa/s DAC conversion rate will significantly reduce effects due to both of these. $\sin x/x$ roll-off is reduced from -4dB to -0.22dB, and the increased oversampling [DAC conversion rate / signal rate] reduces step sizes to give a direct improvement in spurious performance. The limitation of adopting a high DAC conversion rate then becomes data generation.

These issues should be considered when testing the MB86061 and measurements should be obtained at different conversion rates to establish the most appropriate operating conditions for the target application.

For convenience the board has been configured using soldered zero-ohm links as a transformer coupled differential output. To enable single-ended outputs changes to the soldered zero-ohm links would be required. For rise/fall-time tests, the transformer-coupled output should not be used since the transformer response will limit the dV/dt . The DAC current switches are designed to give the best possible differential performance, at the expense of some single ended performance, so there is a noticeable difference between the two configurations. The revised analog output circuit uses an additional transmission line transformer to improve rejection of common-mode distortion at the DAC output.

If a spectrum analyser is used to measure the output spectrum this must have very good noise and distortion, for example HP8562E or R&S FSEA30. In addition, the input attenuator setting should be chosen such that input mixer distortion does not limit the measurements (e.g. 30dB RF attenuation). This implies that narrow resolution bandwidths and/or averaging are required to obtain low enough measurement noise floor.

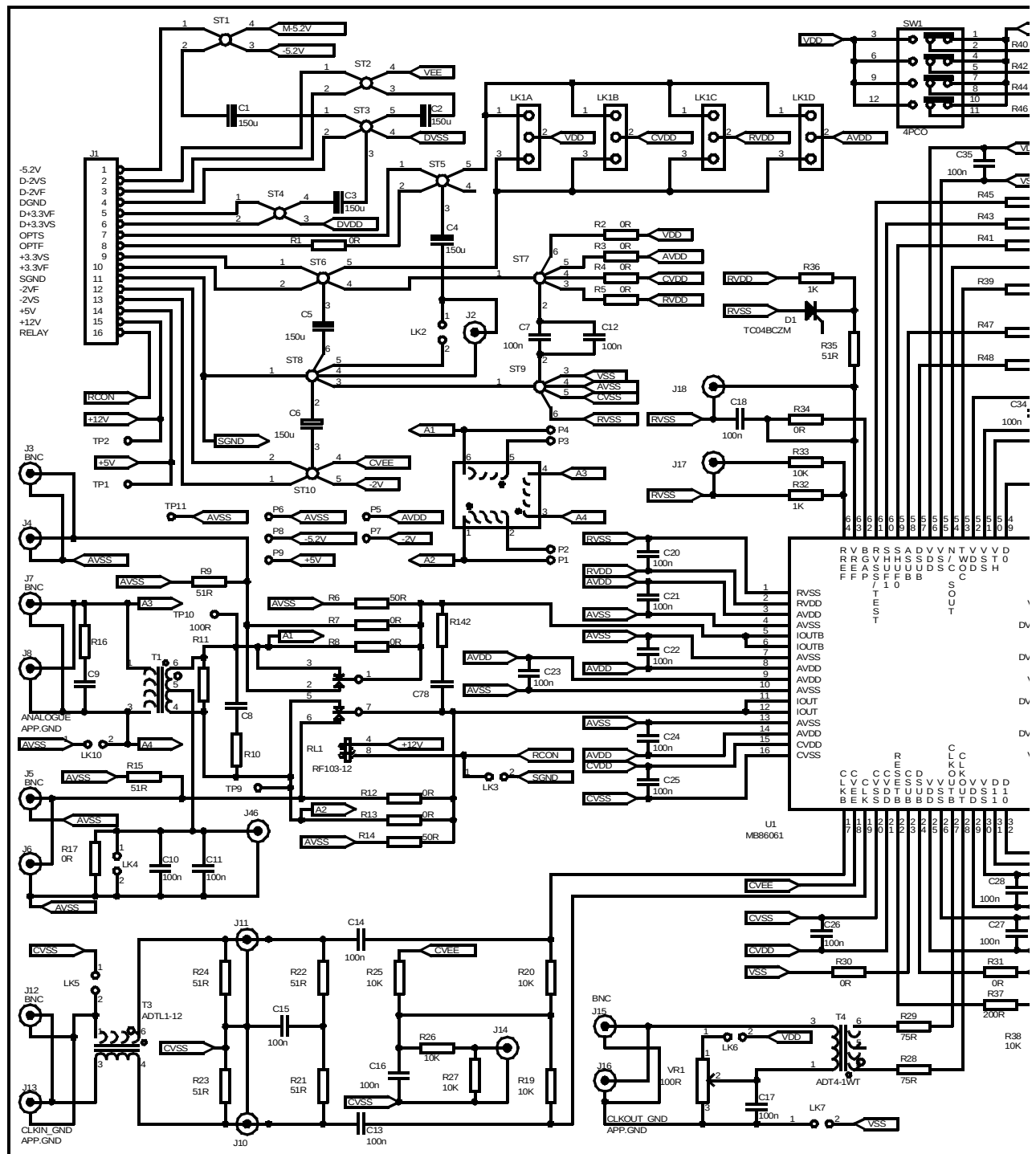
Input data can be generated with an Arbitrary Waveform Generator, for example a Sony/Tektronix AWG520. This can produce 10-bit ECL data (set the digital output to +0.2V to -0.8V) and a data clock. Care should be taken to ensure that the data cables and the clock cable are the same length, so as to avoid any shift in the clock to data timing relationship. However, the phase of the AWGs clock-out may be outside the DACs allowable range. If so, a low noise signal generator such as the Marconi 2042 could be used to provide the clock. This has the facility to adjust the phase of the output signal compared with its frequency standard output (which is driving the AWGs 10MHz reference input).

Appendix A Evaluation Board Circuit Diagrams

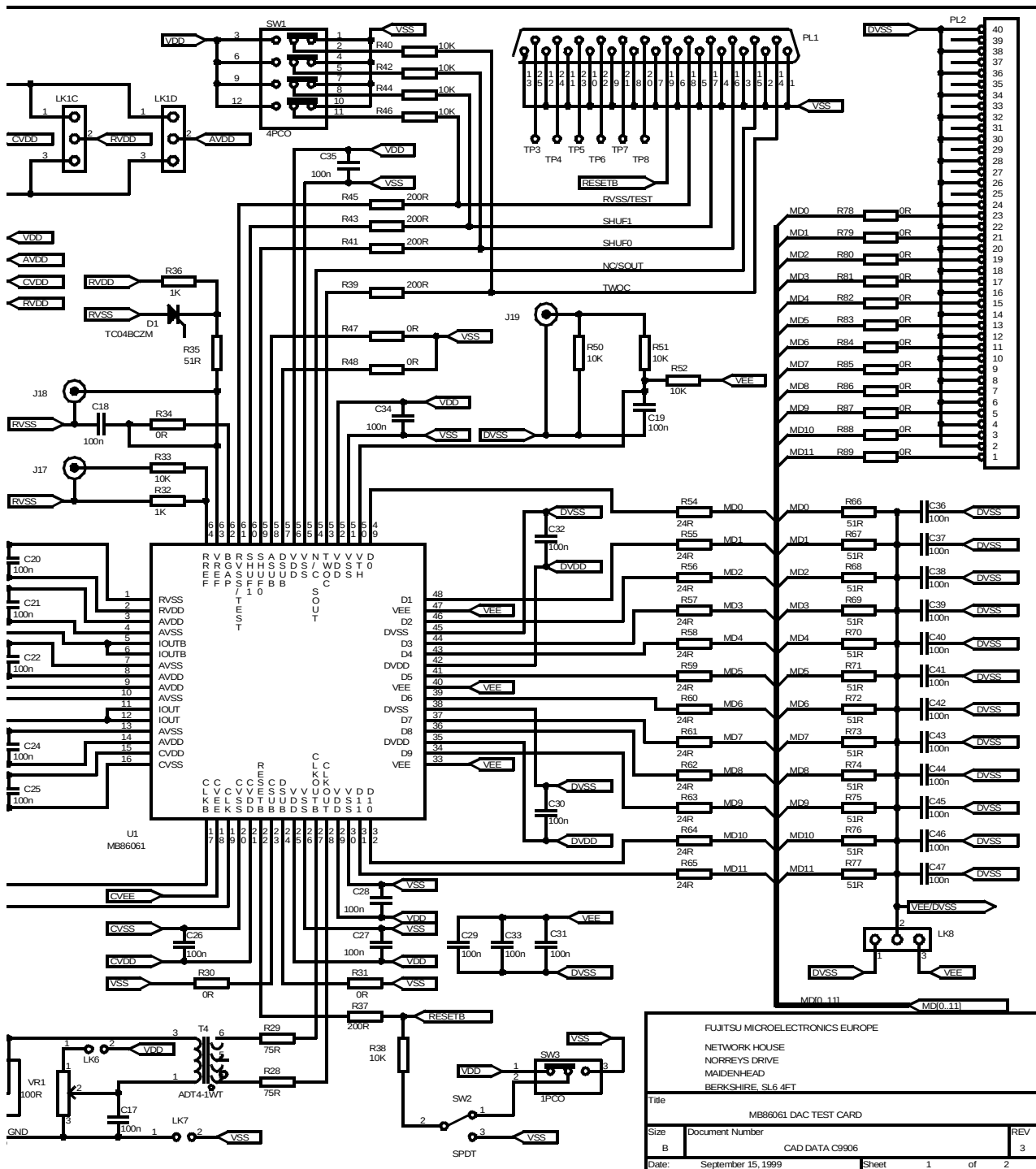
Appendix A shows the circuit diagrams of the DK86061-3 evaluation board. Note that these diagrams are for reference only and that some components fitted to the board may be of a different value to the schematics or not fitted at all. Fujitsu has undertaken to document these changes where possible. The schematic is divided over four pages for clarity. Two 12-bit wide data busses are used to minimize diagram complexity, and are referred to as the Data bus [D0A, D0B to D11A, D11B] and the Multiplexer Data bus [MD0 to MD11].

- Sheet 1 - Main DAC support circuitry, including analog output interfaces [covers 2 pages]
- Sheet 2 - ECL data input multiplexers, including SMA/SMB input data connectors [covers 2 pages]

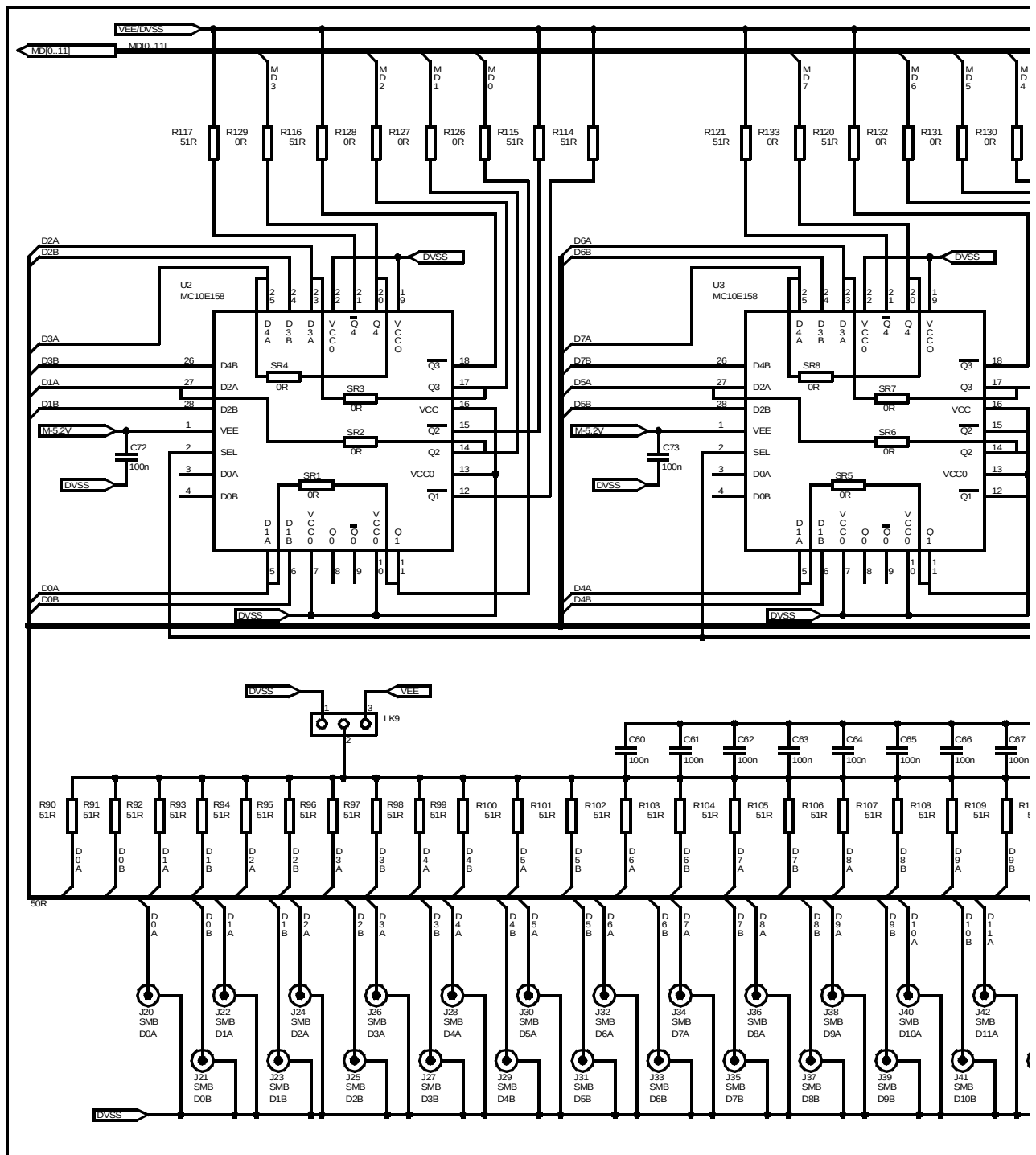
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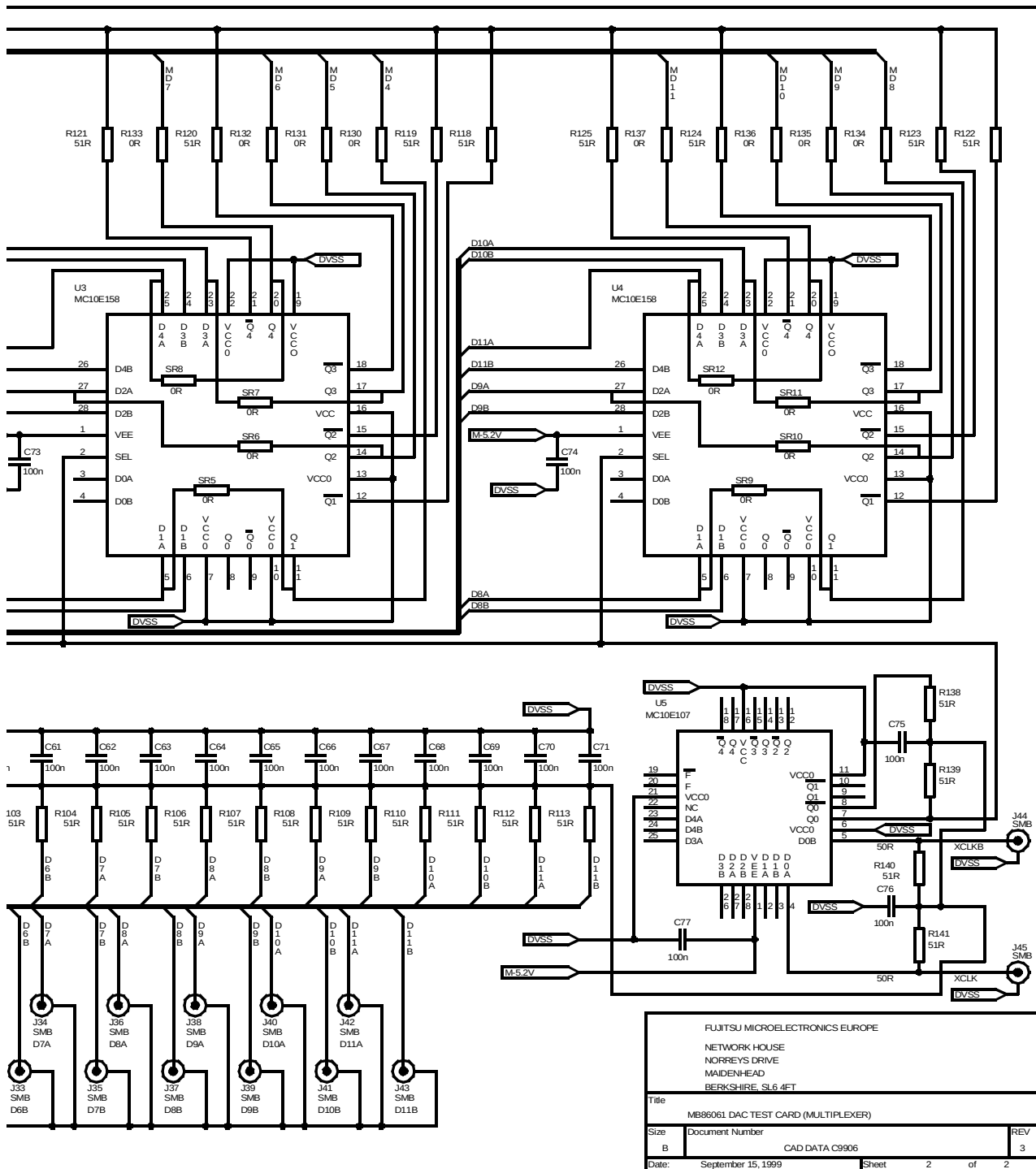
DK86061-3 12-bit 400MSa/s DAC Evaluation Board



DK86061-3 12-bit 400MSa/s DAC Evaluation Board



DK86061-3 12-bit 400MSa/s DAC Evaluation Board



A.1 Components Not Fitted to the PCB

Table A1: Components Not Fitted

Reference	Value	Description
LK1a, b, c, d	-	Power supply selection jumper links
LK2	-	PSRR jumper link
LK3	-	Single-ended output selection jumper link
LK9	-	Input data termination selection jumper link
J2, J4, J6, J8, J10, J11, J13, J14, J16 to J20 to J44 (evens), J45	SMA/SMB	SMA/SMB connectors
J3, J5	BNC	BNC connectors
D1	TC04BCZM	Reference diode
RL1	RF103-12	Output selection relay
C4	150uF	Optional power supply decoupling capacitor
C9, C78	33pF	Analog output RC network capacitors
C60 to C61, C72 to C77	100nF	Decoupling capacitors
R1	0R	Optional power supply PSRR resistor
R7, R12	0R	Single-ended output relay bypass resistors
R9, R13	51R	Single-ended output termination resistors
R16, R132	51R	Analog output RC network resistors
R17	0R	CMRR jumper link bypass resistor
R35	51R	Reference series resistor
R36	1K	Reference current limit resistor
R90 to R113	51R	Input data termination resistors
R126 to R137, SR1 to SR12	0R	Input data multiplexers selection and bypass resistors
R138 to R141	51R	XCLK termination resistors
U2, U3, U4	MC10E158	Input data multiplexers
U5	MC10E107	Input data multiplexer quad XOR
T2	-	Optional analog output circuit transformer

A.2 Changes to PCB Schematics

Table A2: Schematic Changes

Reference	New Value	Description
T1(a)	ADTT1-1	Mini-Circuits 1:1 analog output transformer
T1(b)	ADTL1-12	Mini-Circuits transmission line transformer

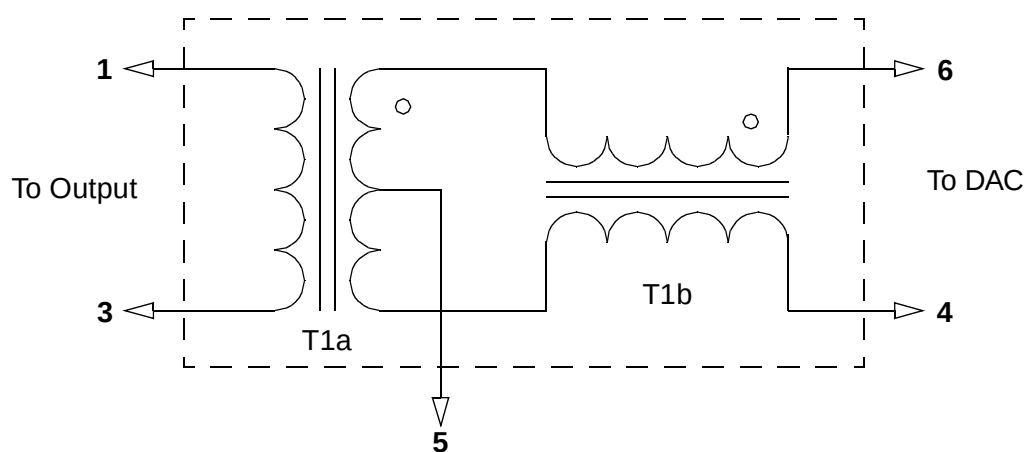


Figure A1 Replacement Schematic For T1 (Pin Numbers Refer To T1)

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Appendix B Component Overlays

II

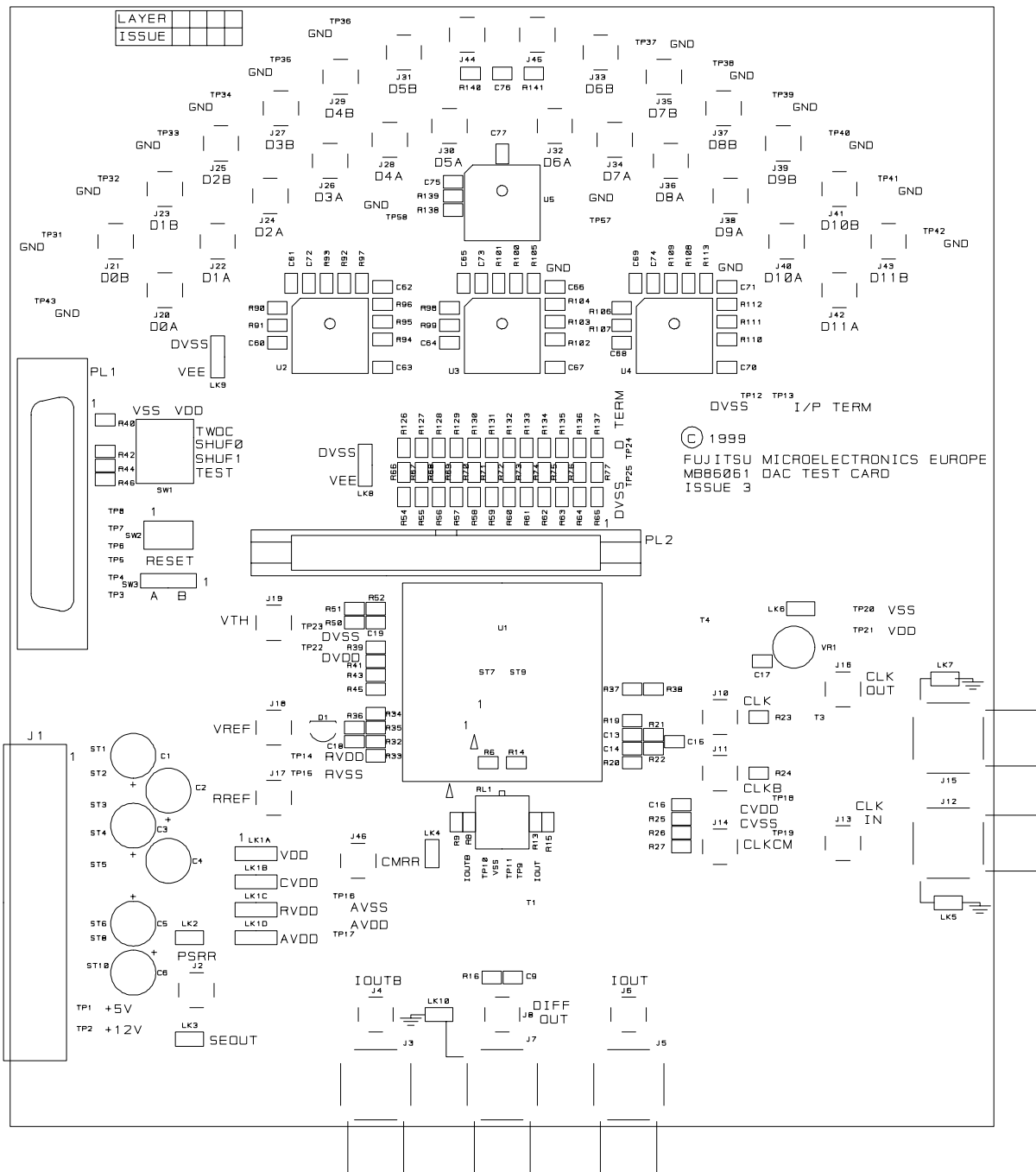


Figure B1 Component Overlay For Layer 1, (Component Side)

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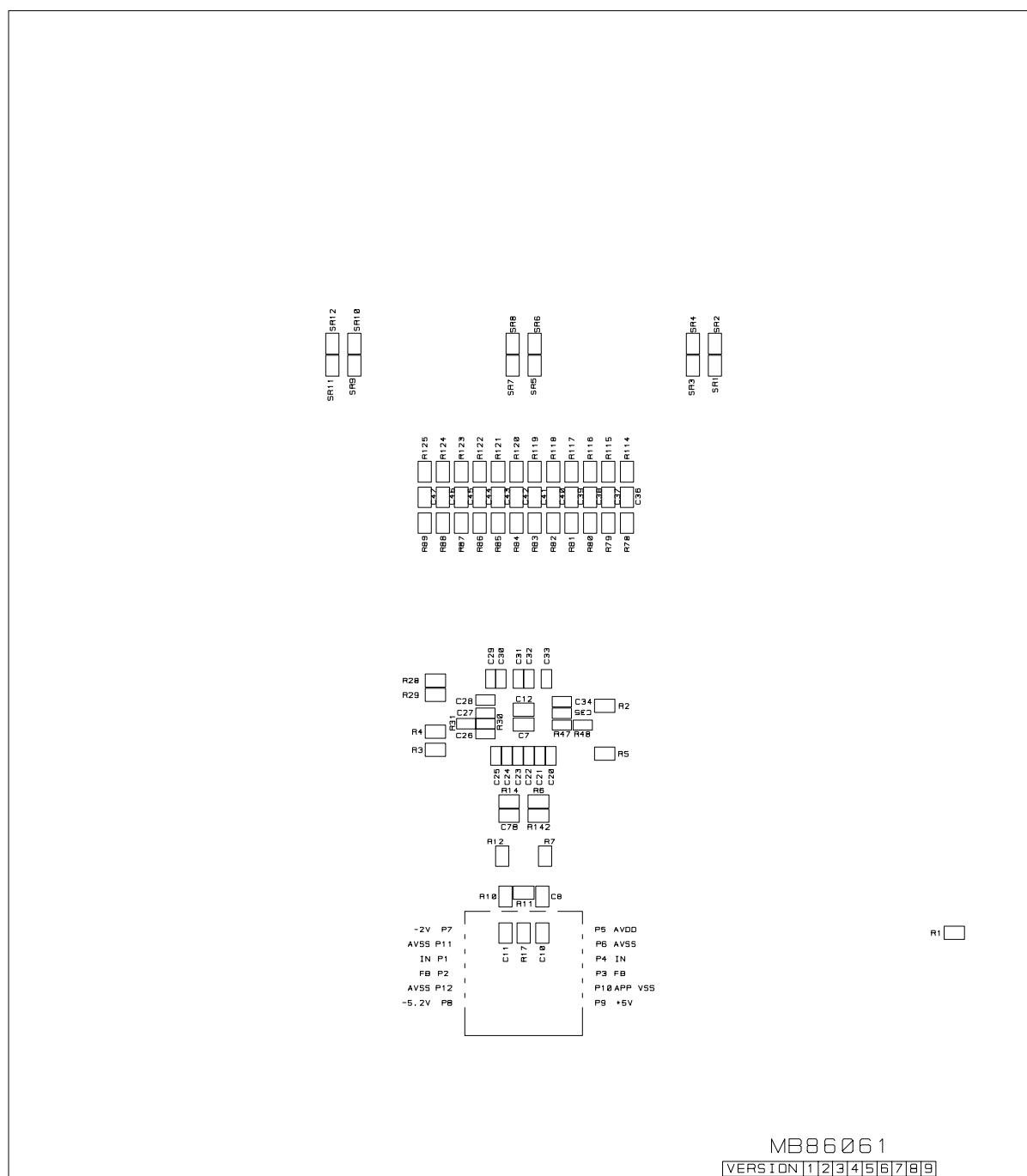
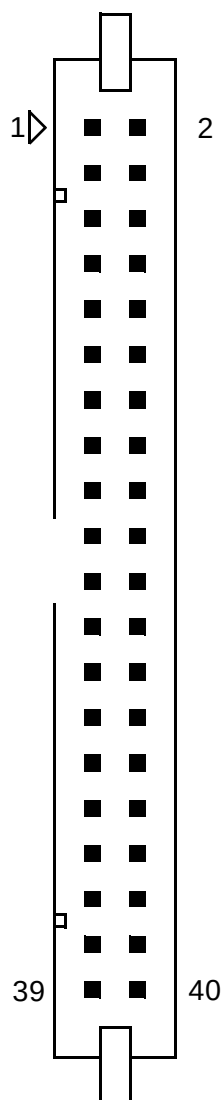


Figure B2 Component Overlay For Layer 4, (Solder Side)

Appendix C Connector Pin Functions

Table C1: Data Connector PL2 Pin Functions



Pin	Function
1	Data Bit 11 (MSB)
3	Data Bit 10
5	Data Bit 9
7	Data Bit 8
9	Data Bit 7
11	Data Bit 6
13	Data Bit 5
15	Data Bit 4
17	Data Bit 3
19	Data Bit 2
21	Data Bit 1
23	Data Bit 0 (LSB)
25	Not Used
27	Not Used
29	Not Used
31	Not Used
33	Not Used
35	Not Used
37	Not Used
39	Not Used
2 to 40 (Even numbers only)	Data Ground (DVSS)

Table C2: Control Connector PL1 Pin Functions

Pin	Function
1 to 13	Digital Ground (VSS)
14	TWOC
15‡	SOUT (O/P)
16	SHUF0
17	SHUF1
18‡	TEST
19	RESETB
20†	Test point 8
21†	Test point 7
22†	Test point 6
23†	Test point 5
24†	Test point 4
25†	Test point 3

† These pins are connected to test points so that connections to the prototype area can be made via the control connector.

‡ These pins are for factory test purposes only.

Appendix D Prototype Area

A prototype area has been introduced into the DK86061-3 development kit PCB. This area takes the form of a matrix of pads with plated through holes on a 2.54mm pitch. The pads are made square to allow for 0805 format surface mount devices to be fitted between adjacent pads. The matrix area has four rows individually linked together to act as power rails. These rows are arranged as two pairs, with connections to the internal planes (layers 2 and 3) made to each of the rows. The internal plane regions only occupy the prototype area, and are not linked to any other area of the PCB. The prototype area layout is shown in Figure D1.

Layer 2 would typically be used as the ground plane, and layer 3 as the power plane, with signals routed on layer 1. However the choice in the prototype area is free as the planes are entirely separate to the rest of the PCB.

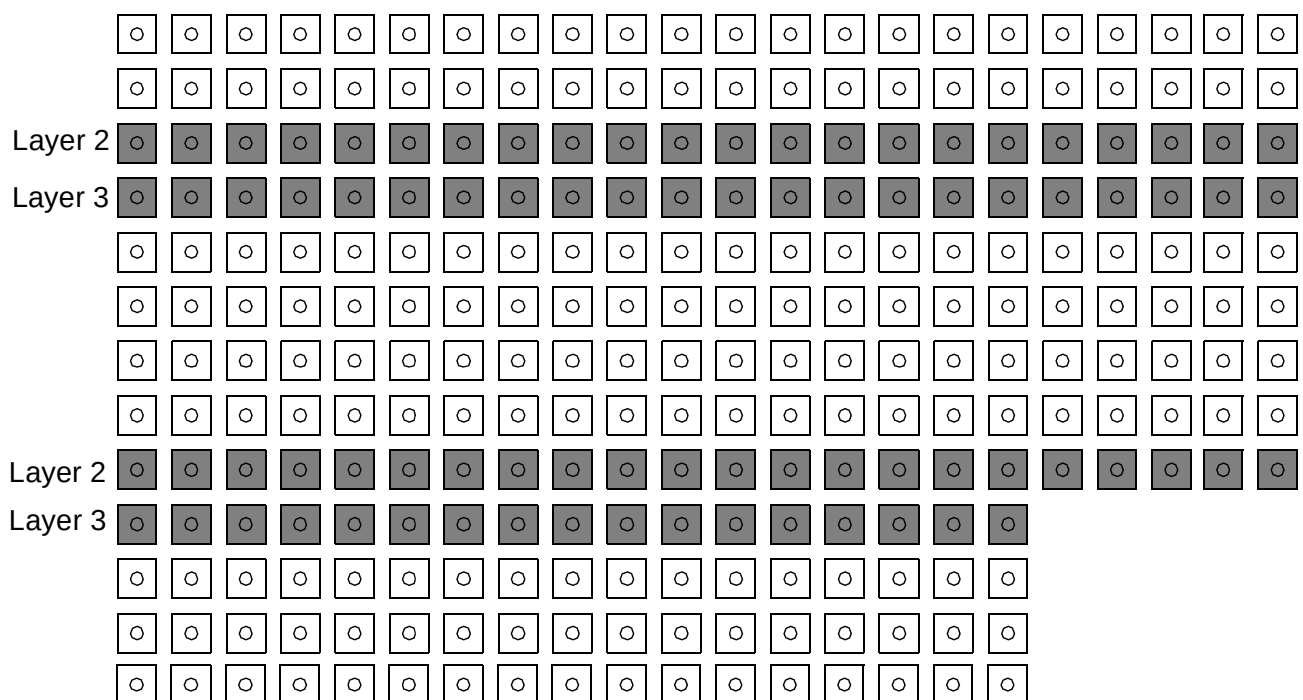


Figure D1 Prototype Area Layout

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